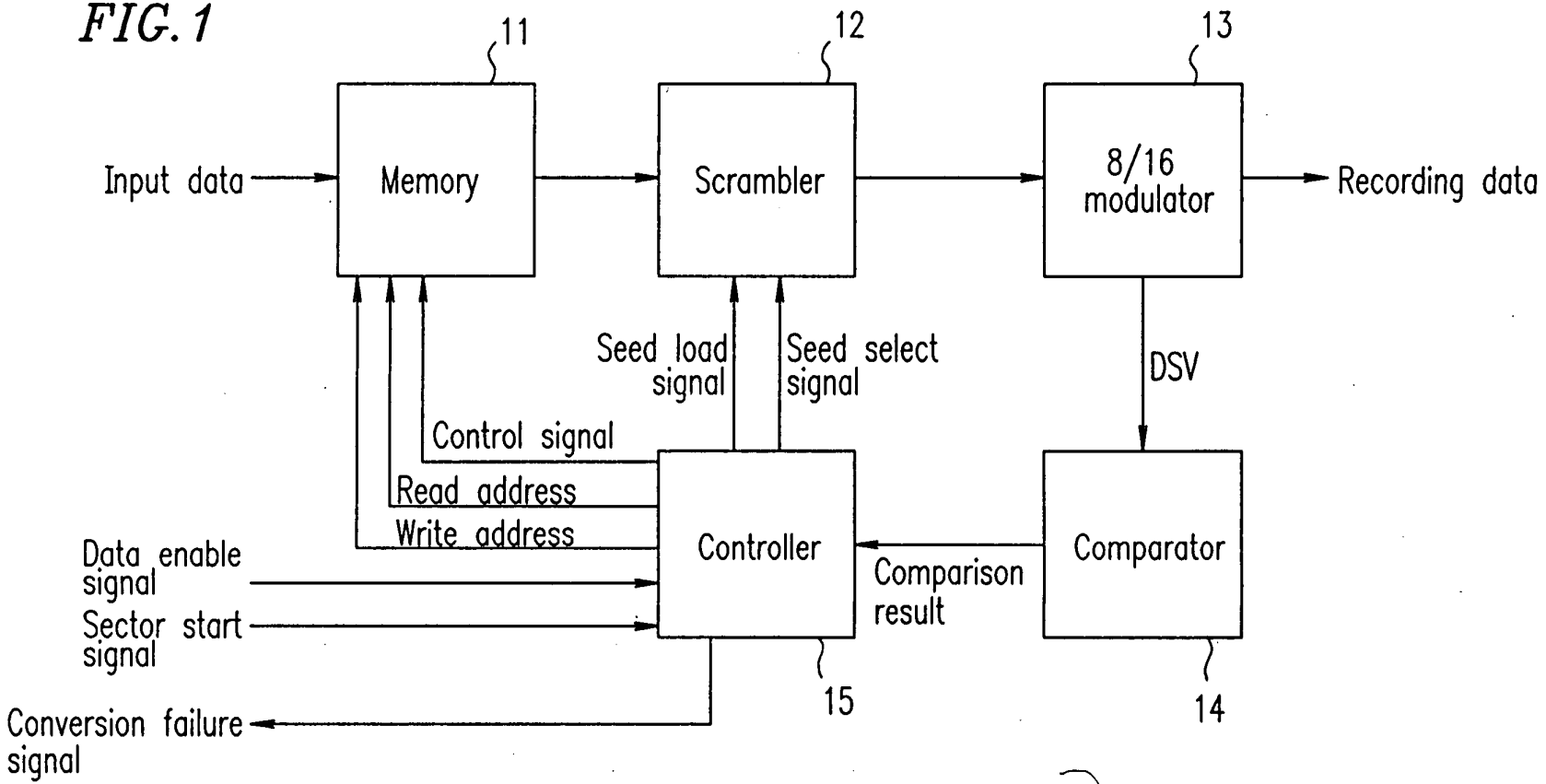
APPROVED BY DRAFTSMAN | O.G. FIG. 1 | CLASS 341 | SUBCLASS 58

FIG. 1



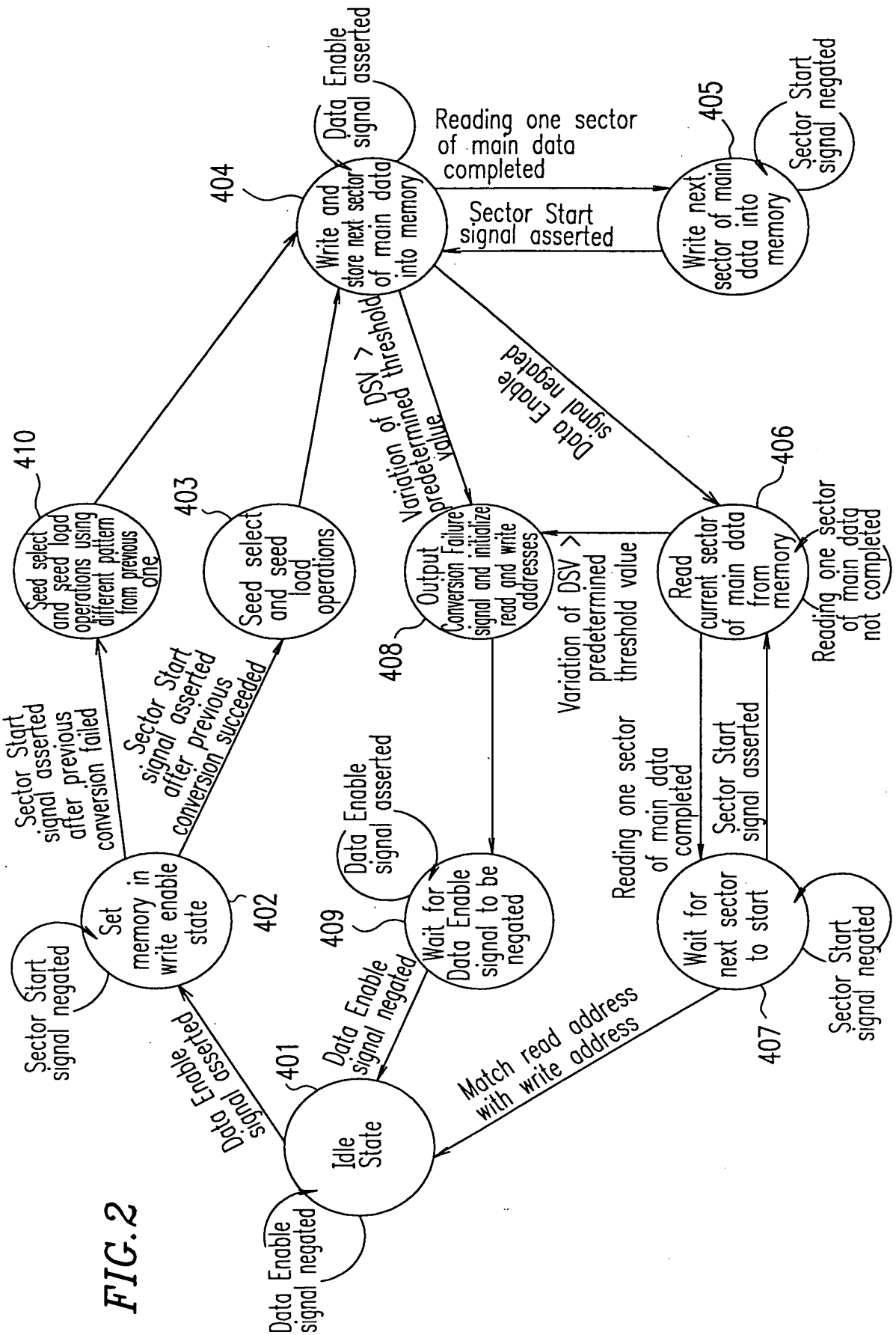

Idle State
401
Set memory in write enable state
402
Seed select and seed load operations
403
Write and store next sector of main data into memory
404
Write next sector of main data into memory
405
Read current sector of main data from memory
406
Wait for next sector to start
407
Output Conversion Failure signal and initialize read and write addresses
408
Wait for Data Enable signal to be negated
409
Seed select and seed load operations using different pattern from previous one
410
Data Enable signal asserted
Data Enable signal negated
Sector Start signal asserted
Sector Start signal negated
Reading one sector of main data completed
Reading one sector of main data not completed
Variation of DSV > predetermined threshold value
Data Enable signal negated
Sector Start signal asserted after previous conversion succeeded
Sector Start signal asserted after previous conversion failed
Data Enable signal asserted
Match read address with write address

FIG.2

BY
DRAFTSMAN
O.G. FIG.
CLASS
SUBCLASS

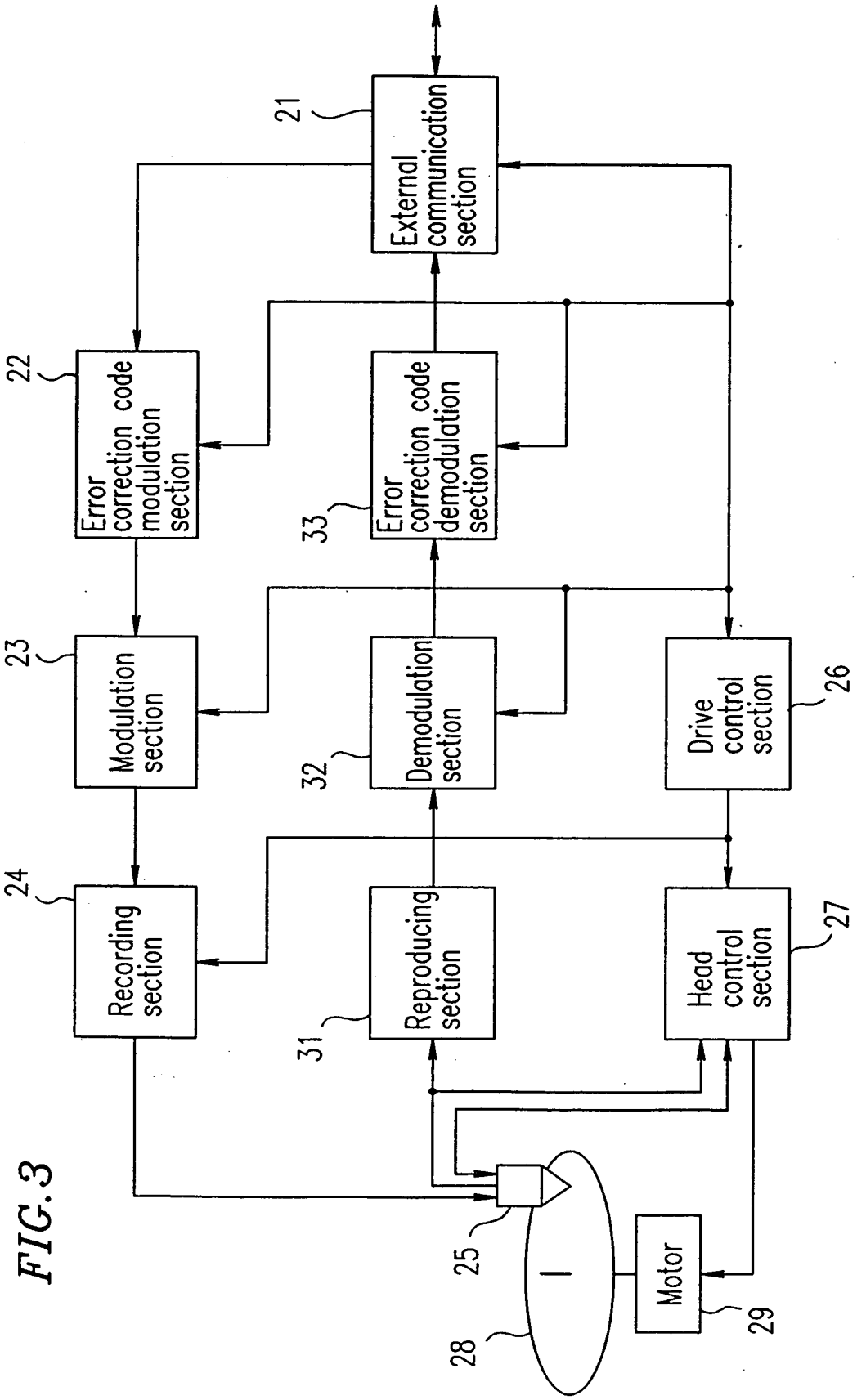


FIG. 3

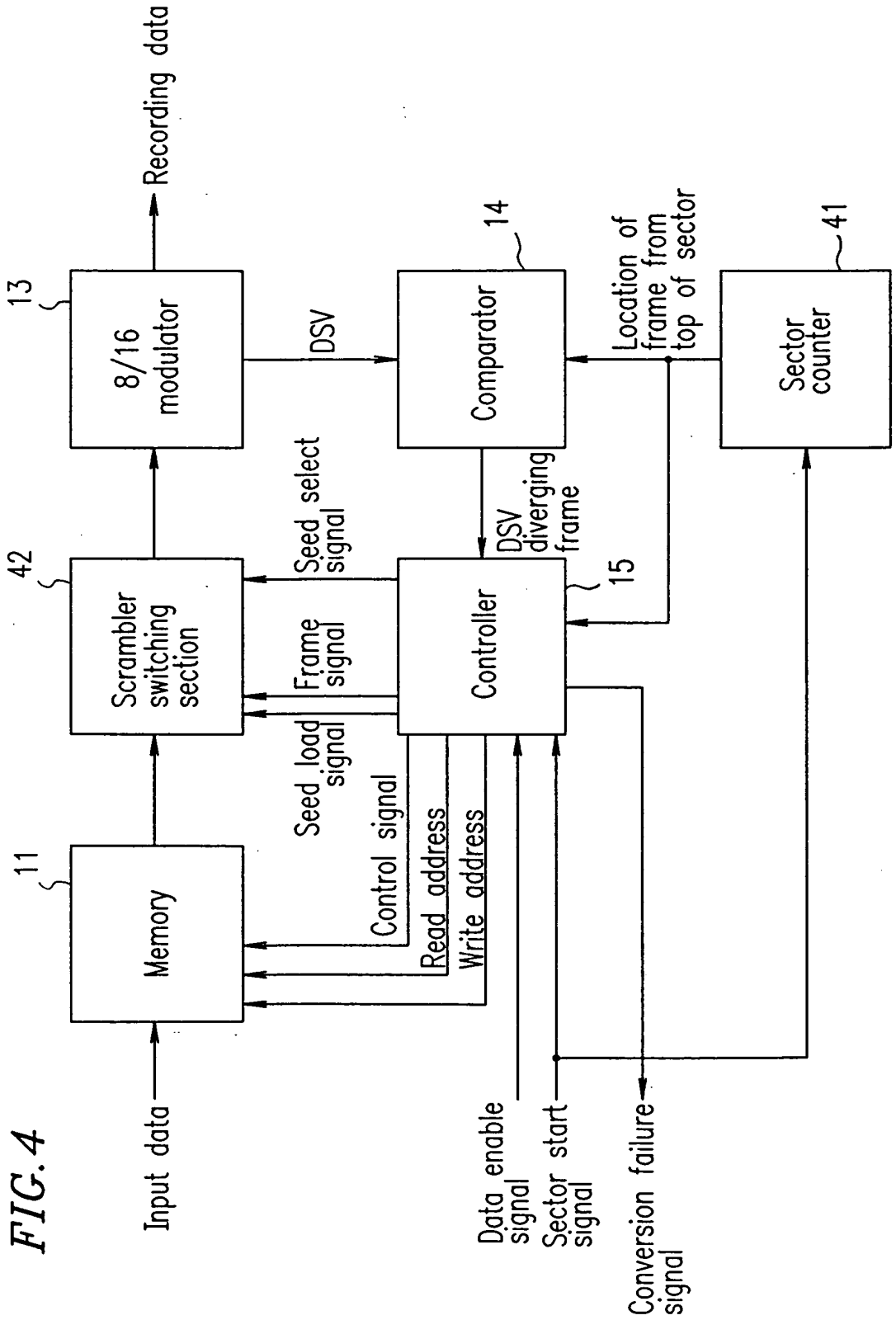

Input data
Memory
11
Scrambler switching section
42
8/16 modulator
13
Recording data
Comparator
14
Controller
15
Sector counter
41
DSV
Location of frame from top of sector
DSV diverging frame
Seed select signal
Frame signal
Seed load signal
Control signal
Read address
Write address
Data enable signal
Sector start signal
Conversion failure signal

FIG. 4

O.G. FIG.
BY
CLASS
SUBCLASS
DRAFTSMAN

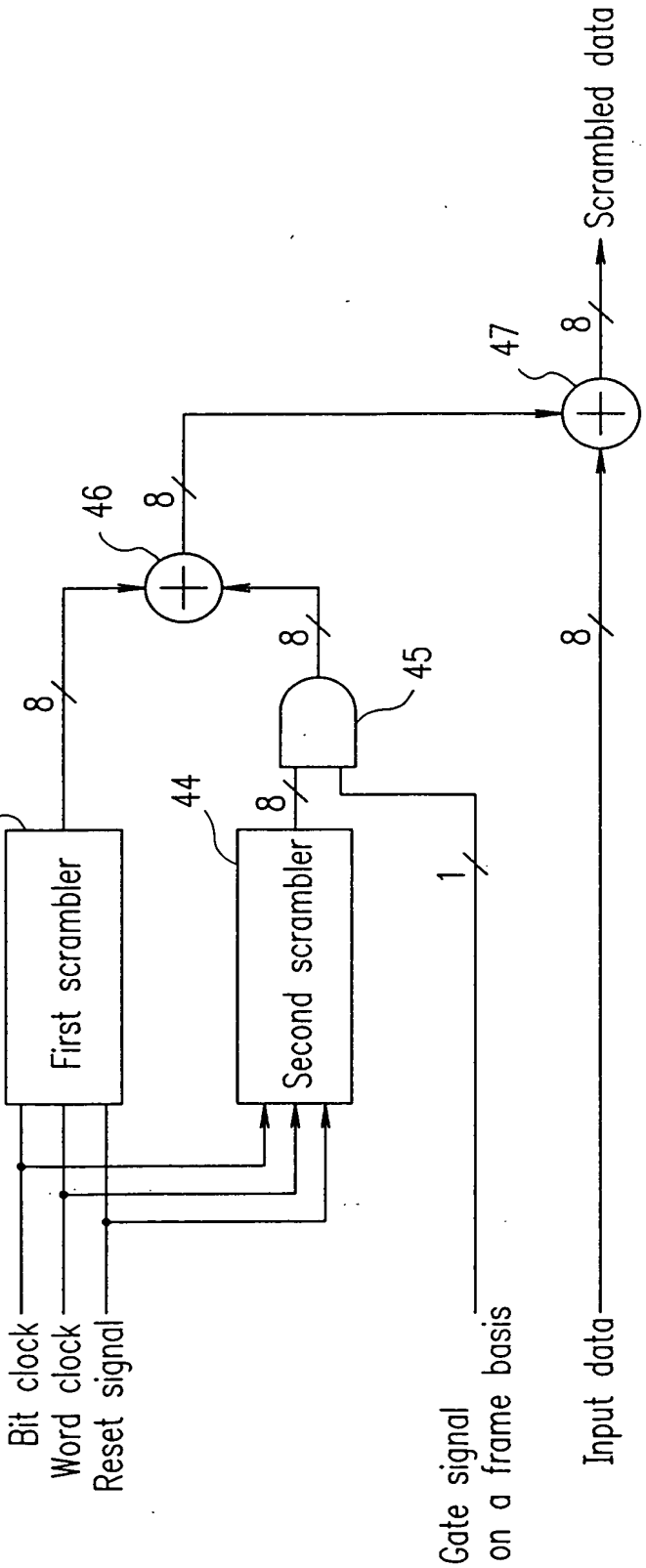


FIG.5

BY | CLASS | SUBCLASS
DRAFTSMAN

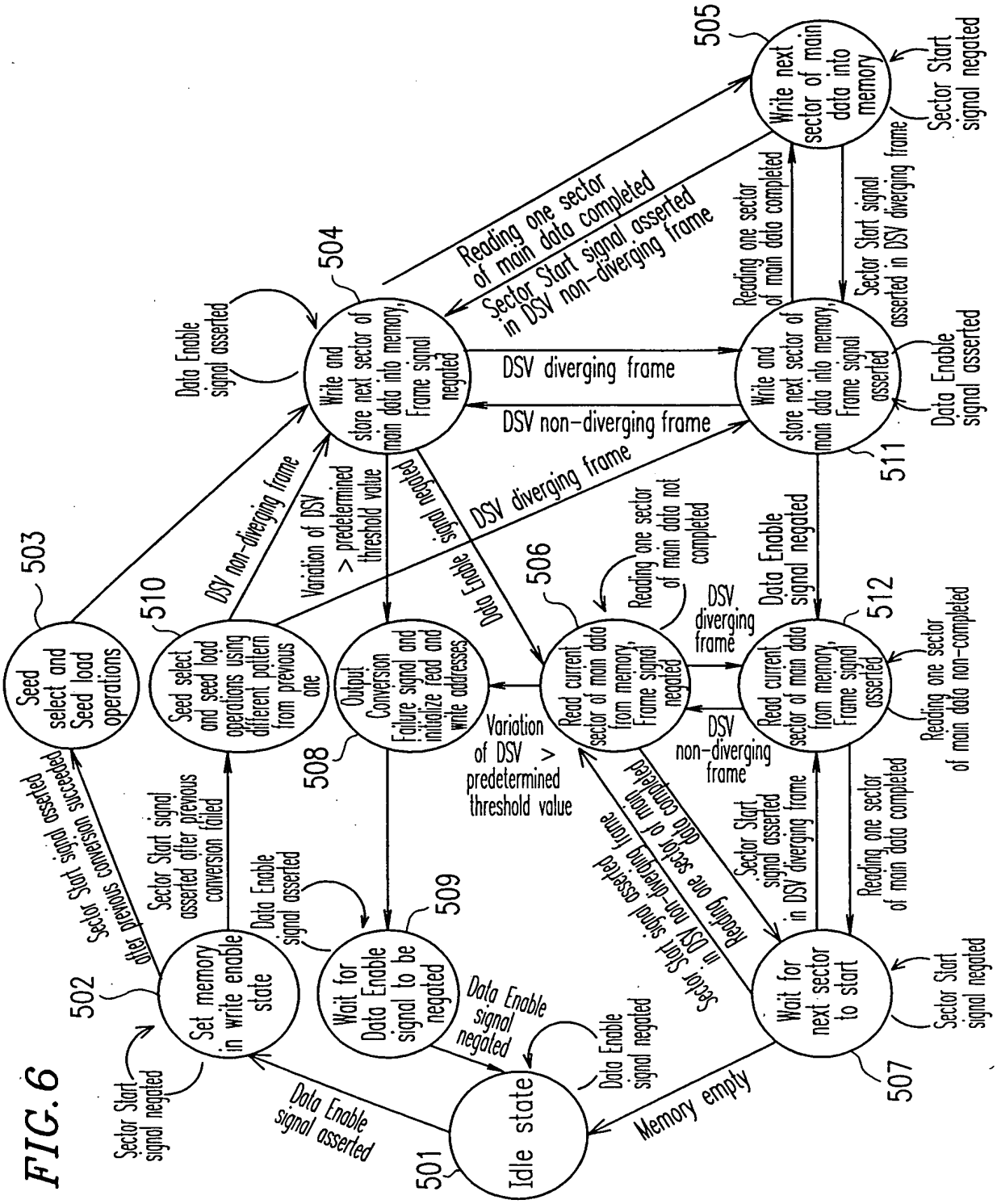


FIG. 6

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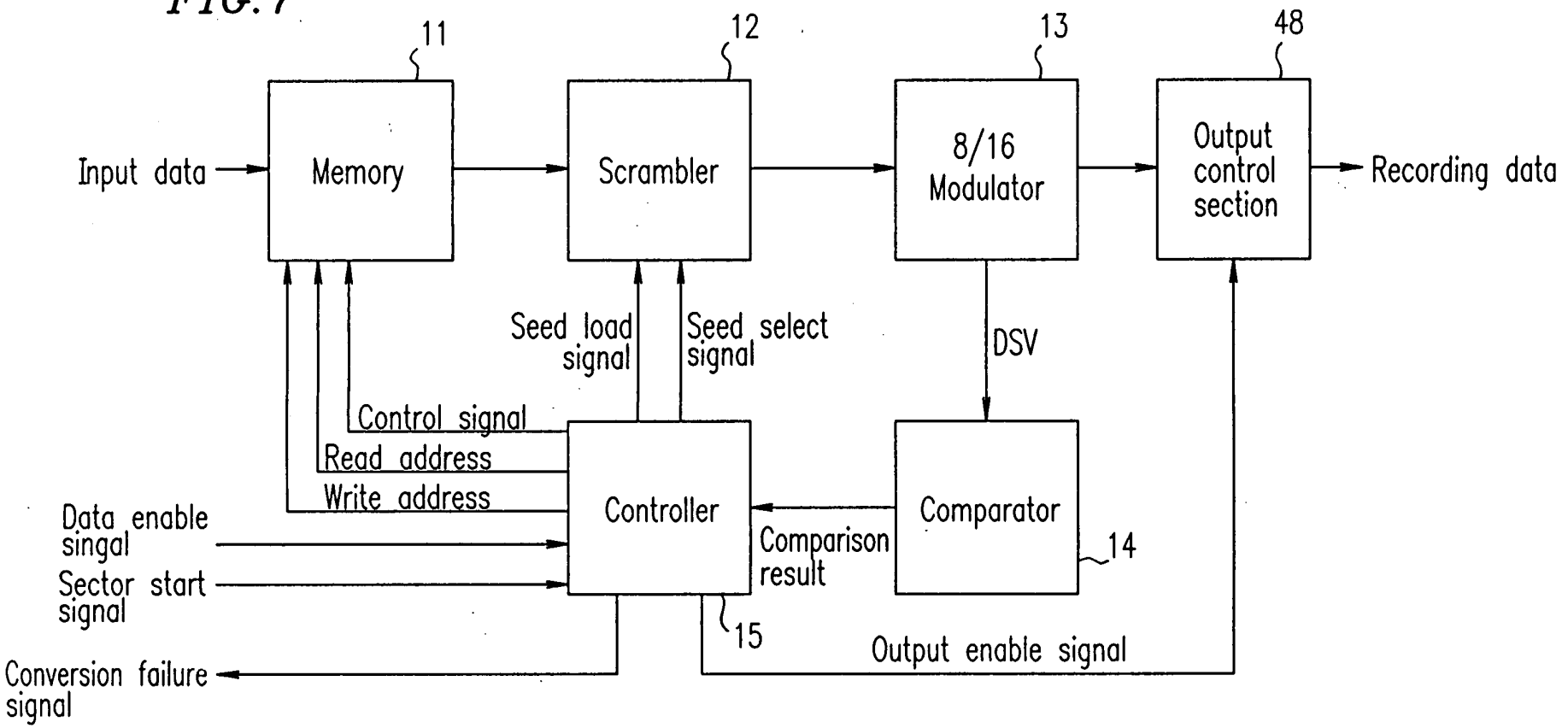
O.G. FIG.
BY
DRAFTSMAN
CLASS
SUBCLASS

FIG. 7



P15105

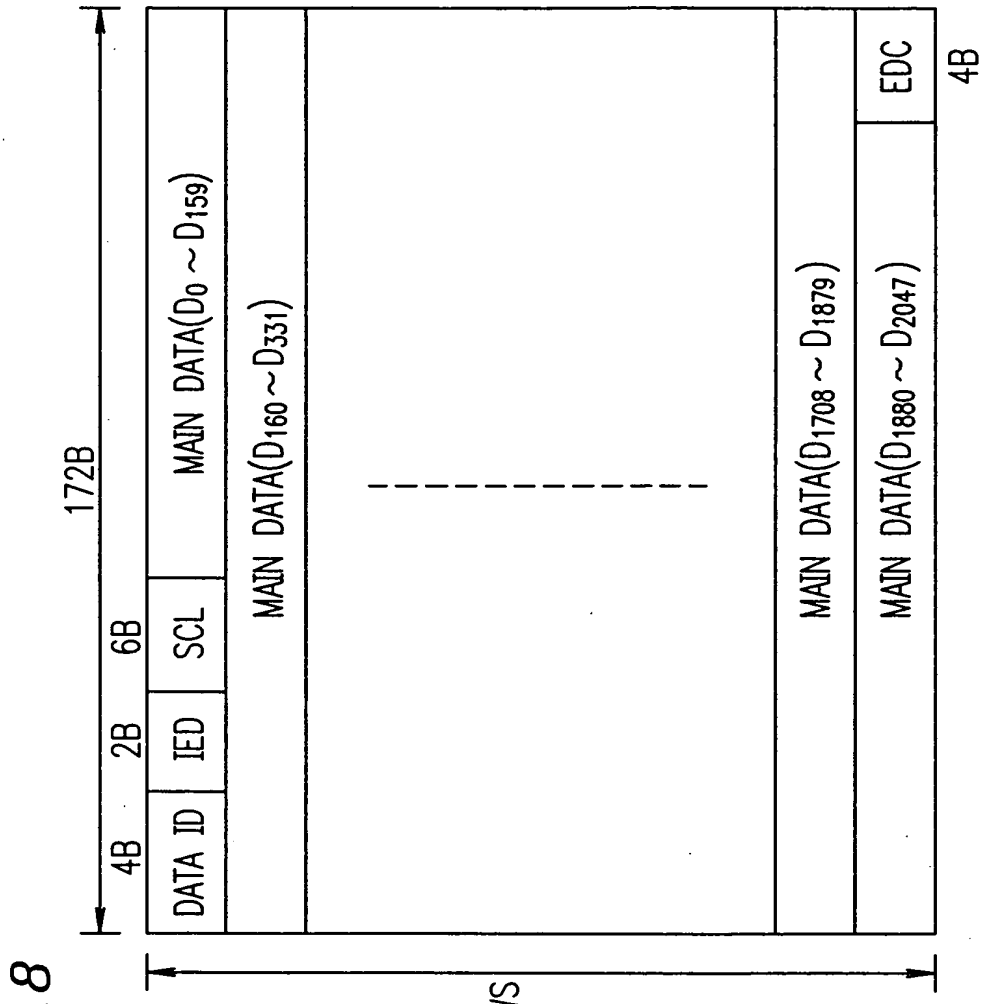
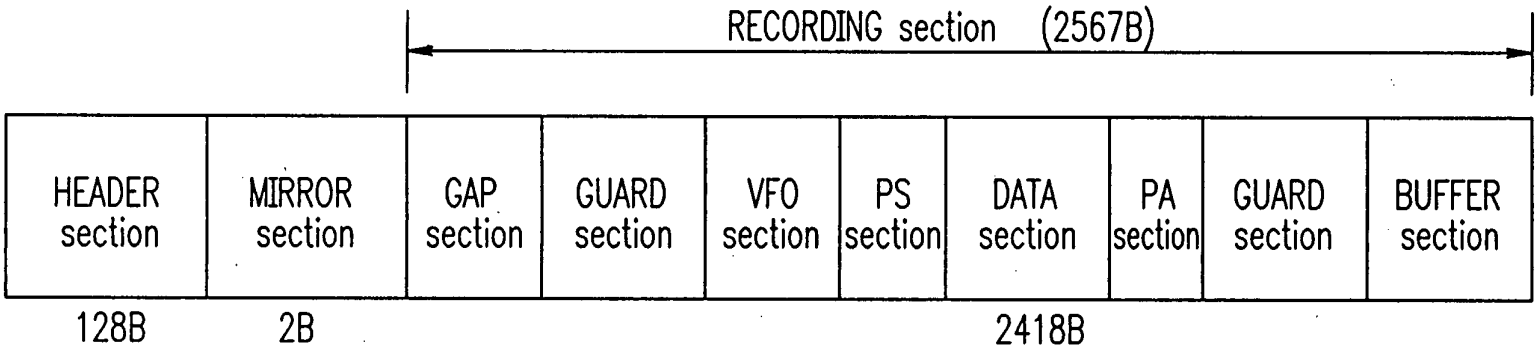

172B
4B
2B
6B
DATA ID
IED
SCL
MAIN DATA($D_0 \sim D_{159}$)
MAIN DATA($D_{160} \sim D_{331}$)
MAIN DATA($D_{1708} \sim D_{1879}$)
MAIN DATA($D_{1880} \sim D_{2047}$)
EDC
4B
12
ROWS

FIG. 8

O.G. FIG.
BY DRAFTSMAN
CLASS SUBCLASS

FIG. 9



O.G. FIG.
BY
CLASS
SUBCLASS

FIG. 10

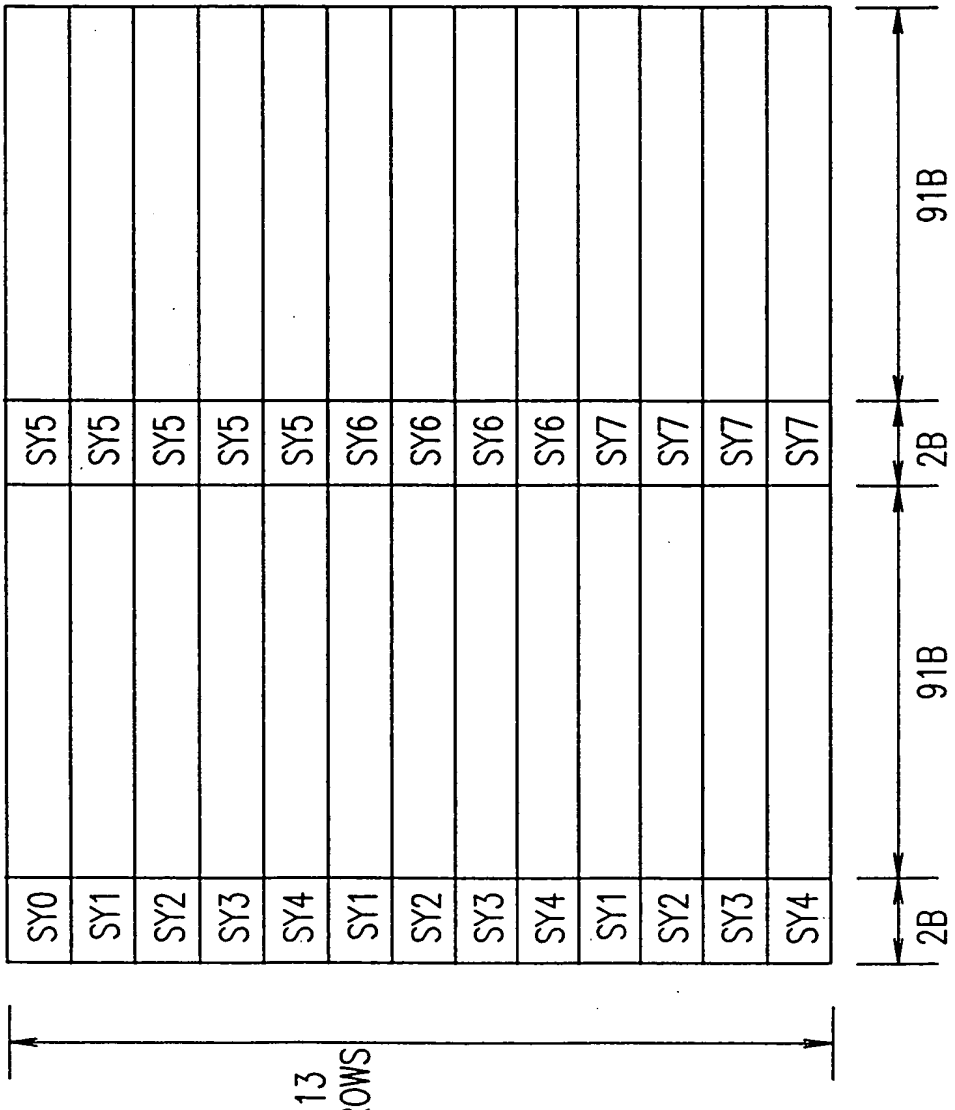
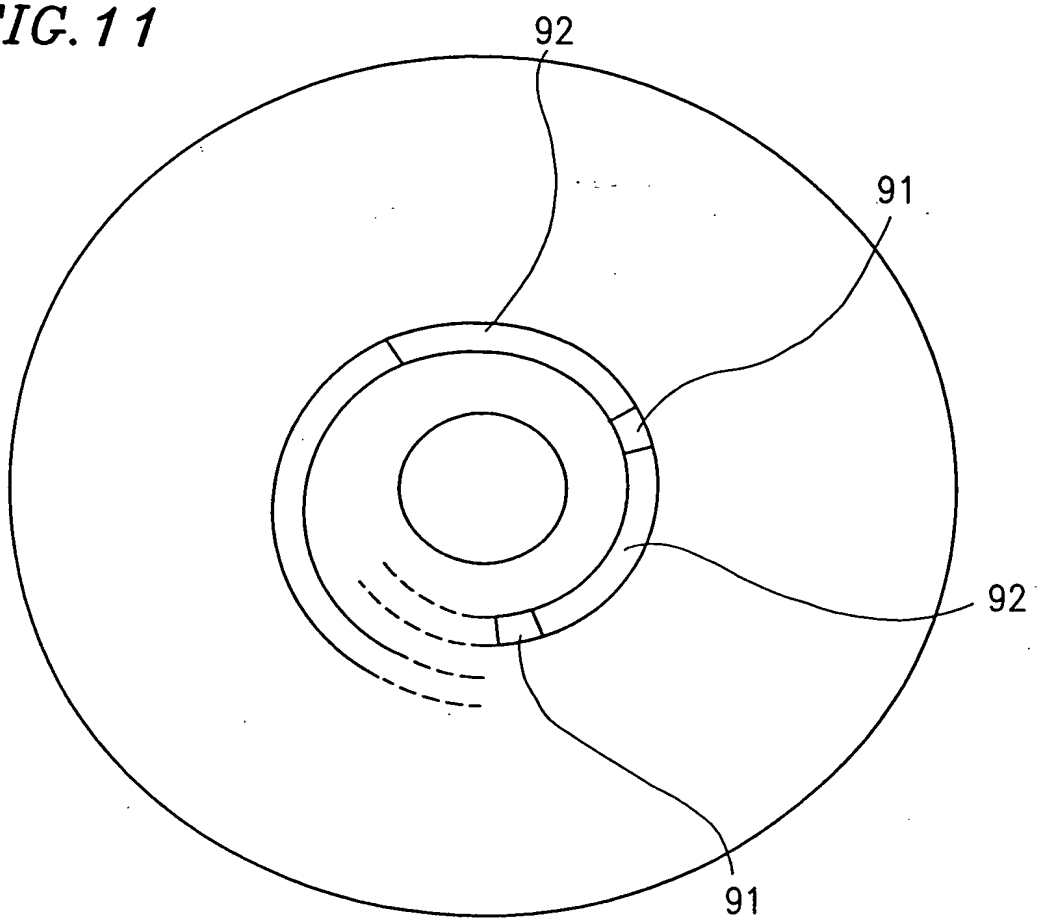


FIG. 11



O.G. FIG.
CLASS
SUBCLASS
BY
DRAFTSMAN

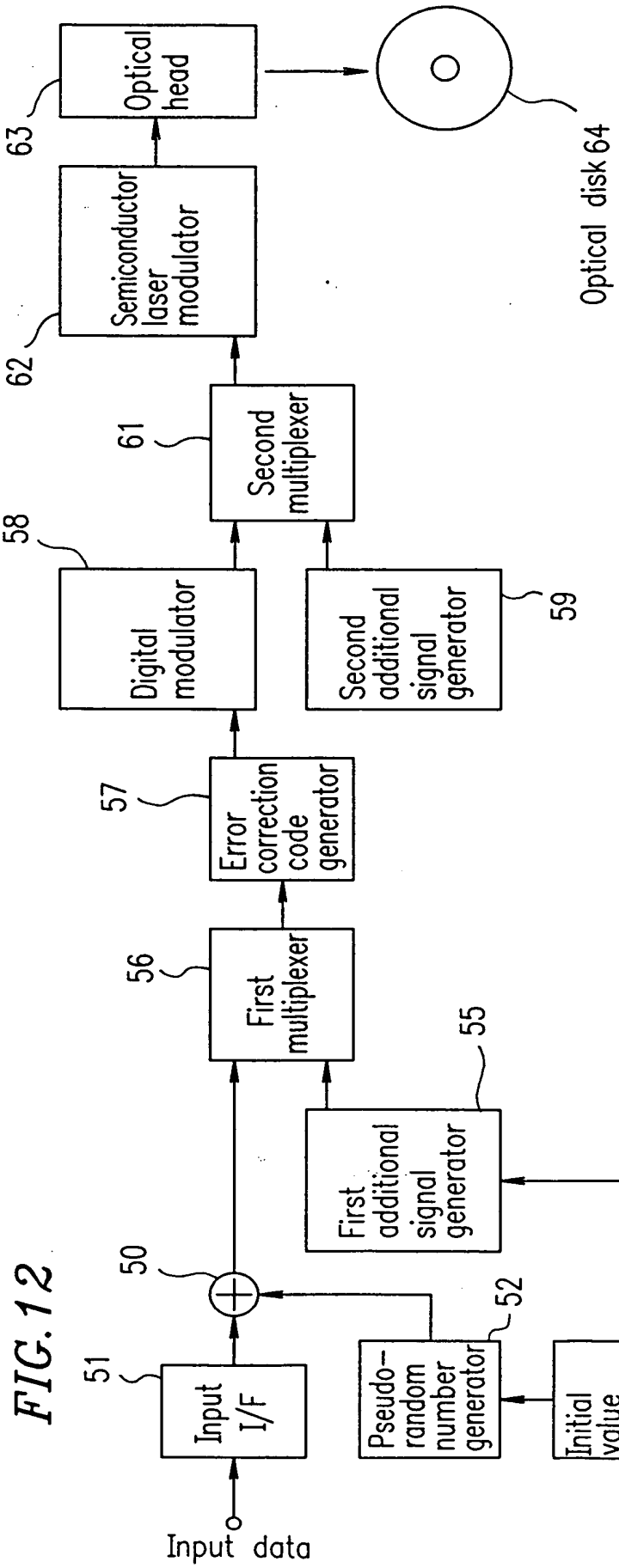

Input data
Input I/F
51
50
Pseudo-random number generator
52
Initial value data generator
53
System controller
54
First additional signal generator
55
First multiplexer
56
Error correction code generator
57
Digital modulator
58
Second additional signal generator
59
Second multiplexer
61
Semiconductor laser modulator
62
Optical head
63
Optical disk 64

FIG. 12

APPROVED
BY
DRAFTSMAN
O.G. FIG.
CLASS
SUBCLASS

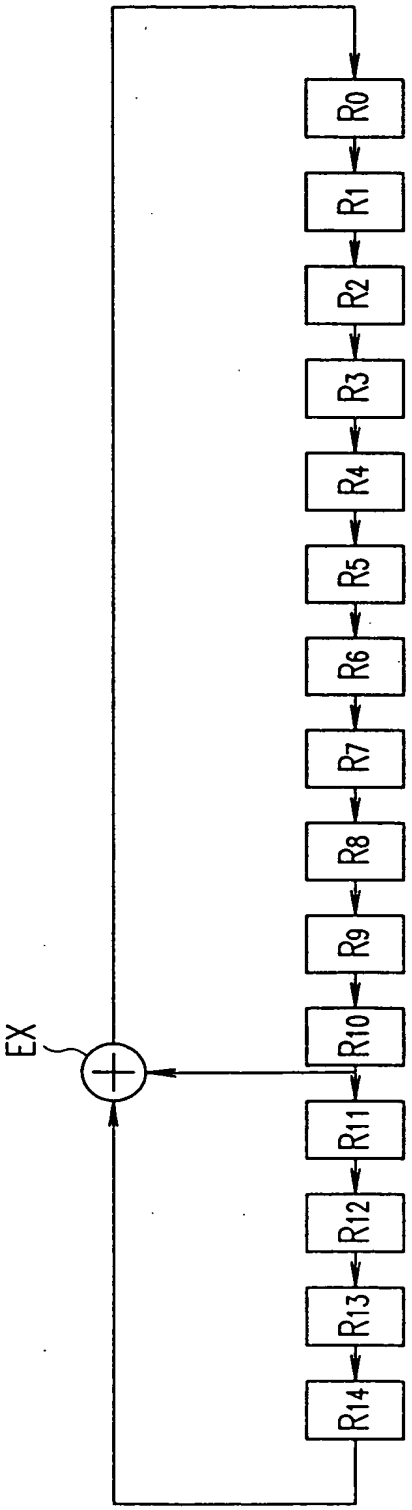


FIG. 13

FIG. 14

Bit string	Initial value
0h	0001h
1	5500
2	0002
3	2A00
4	0004
5	5400
6	0008
7	2800
8	0010
9	5000
A	0020
B	2001
C	0040
D	4002
E	0080
F	0005

O.G. FIG. CLASS SUBCLASS BY EASTMAN

O.G. FIG.
BY DRAFTSMAN | CLASS | SUBCLASS

FIG. 15

Bit string \ Initial value	Rewrite repetition times 0	Rewrite repetition times 1	Rewrite repetition times 2	------	Rewrite repetition times 15
0h	0001h	0090h	0003h	------	0031h
1	5500	3C00	2400	------	2000
2	0002	00A0	0005	------	0032
3	2A00	1E00	1200	------	1600
4	0004	00C0	0006	------	0034
5	5400	3B00	2300	------	2B00
6	0008	00F0	0007	------	0038
7	2800	1D00	1100	------	1300
8	0010	0009	0030	------	0013
9	5000	3A00	2500	------	2A00
A	0020	000A	0050	------	0023
B	2001	1003	3001	------	2007
C	0040	0000	0060	------	0043
D	4002	2006	6002	------	400E
E	0080	000F	0070	------	0083
F	0005	00A3	0052	------	00A2

O.G. FIG.
CLASS
SUBCLASS
BY DRAFTSMAN

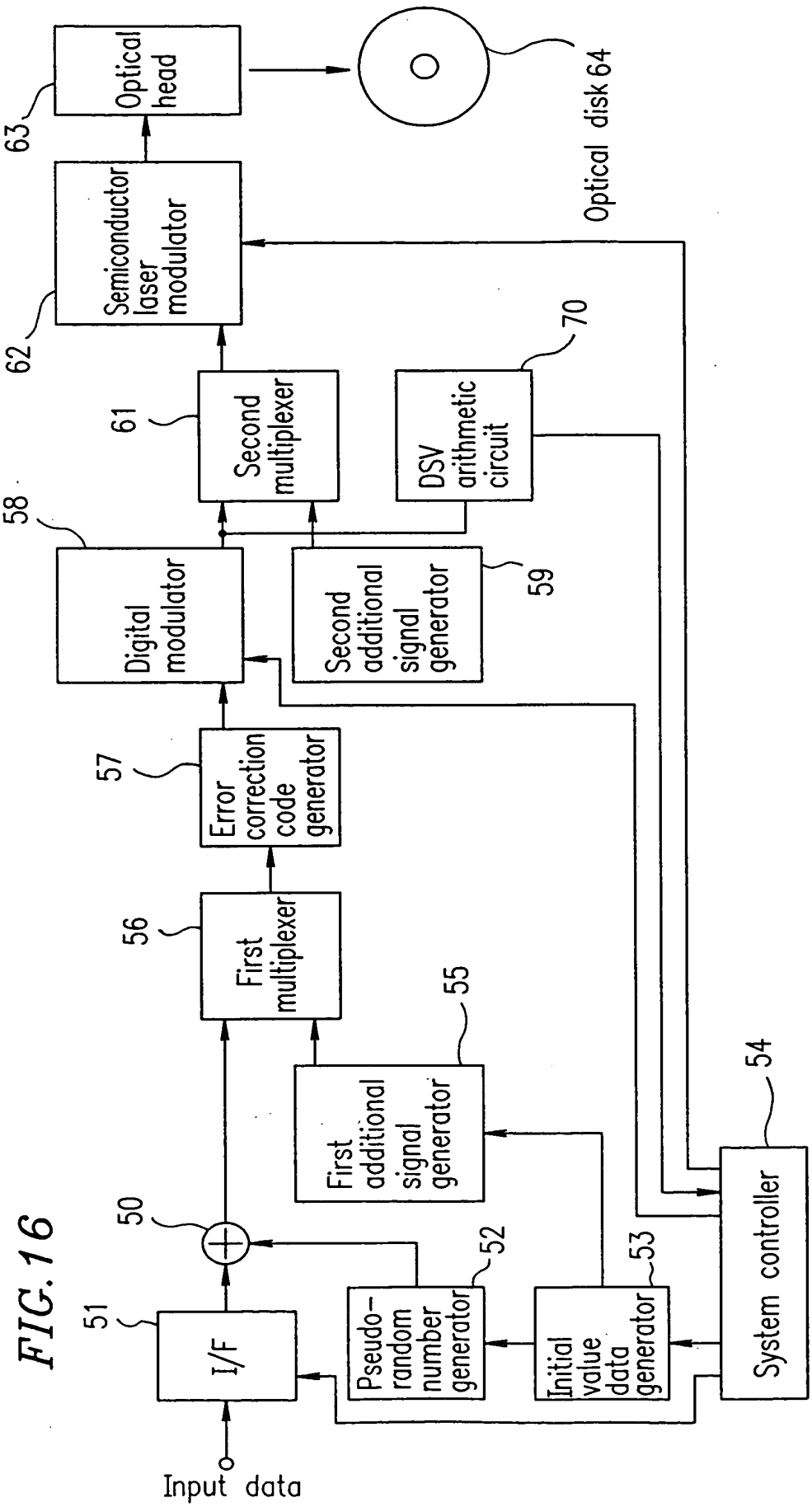


FIG. 16

O.G. FIG.
CLASS
SUBCLASS
BY
DRAFTSMAN

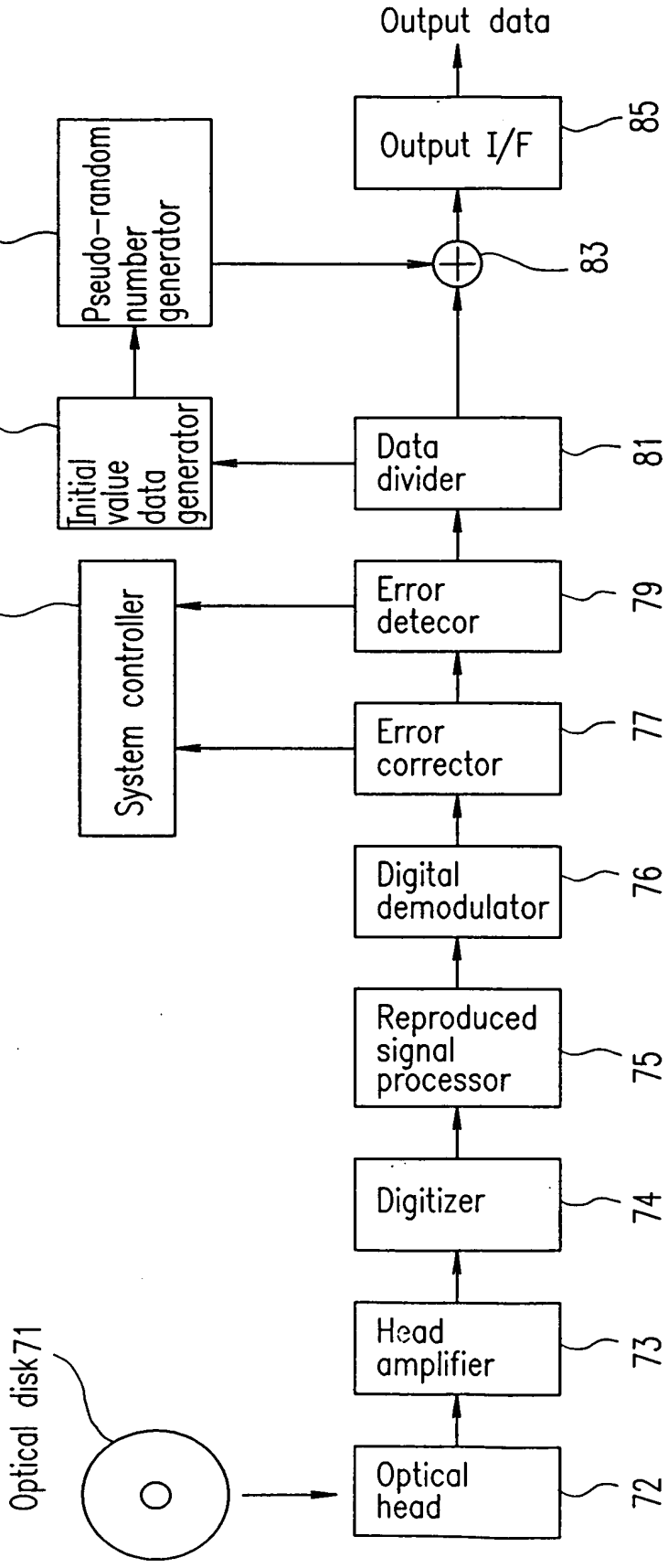


FIG. 17

DRAFTSMAN BY CLASS SUBCLASS

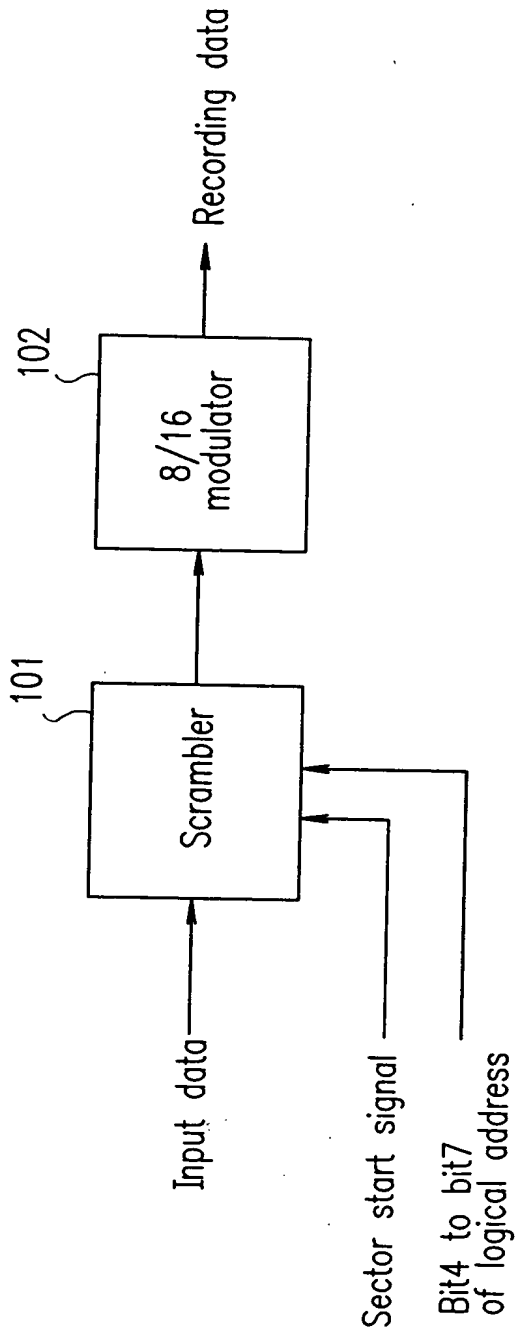


FIG. 18

O.G. FIG.
CLASS SUBCLASS
BY DRAFTSMAN

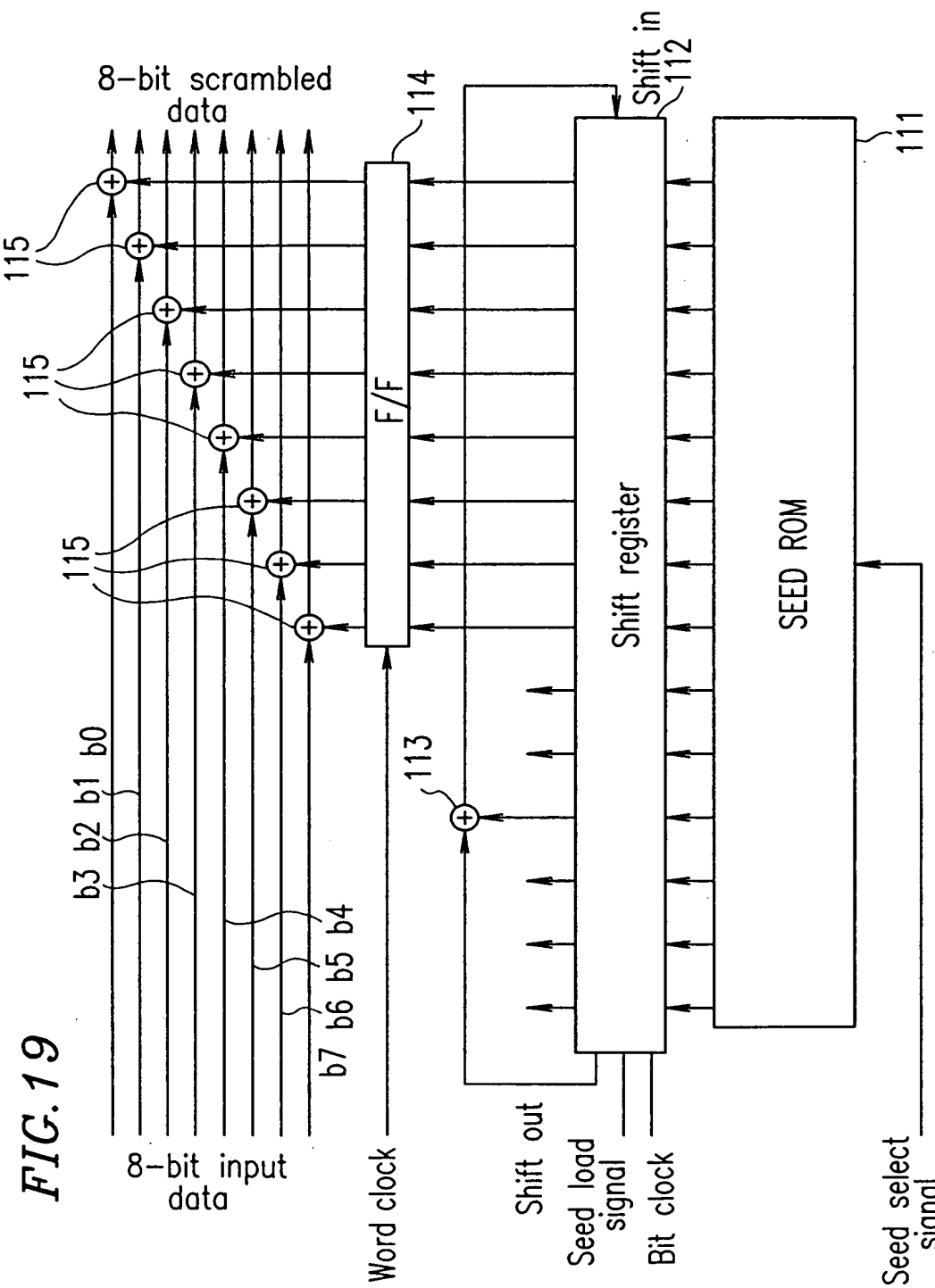
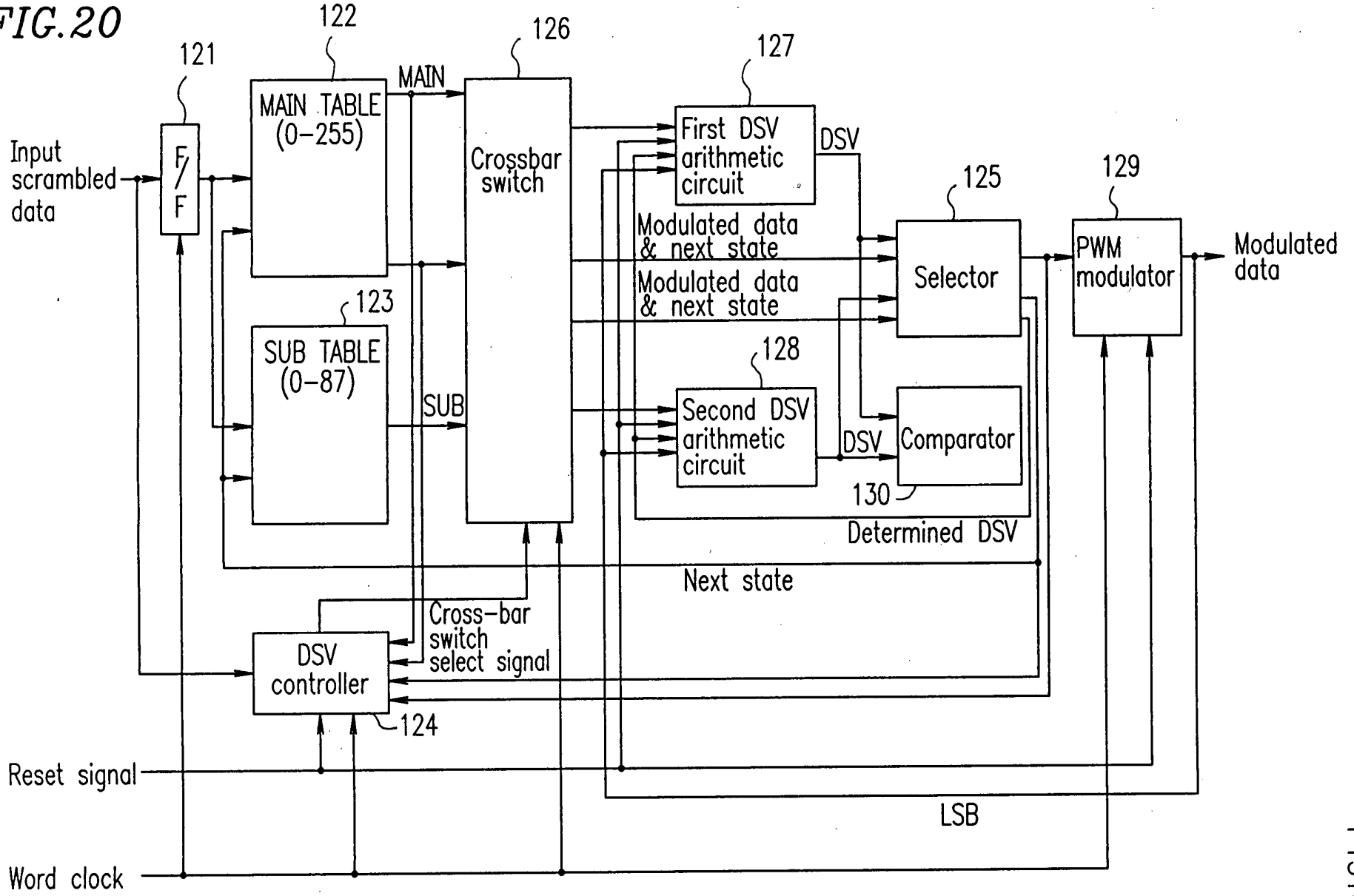


FIG. 19

Q.G. Fig.
BY DRAFTSMAN
CLASS SUBCLASS

FIG.20



P15105

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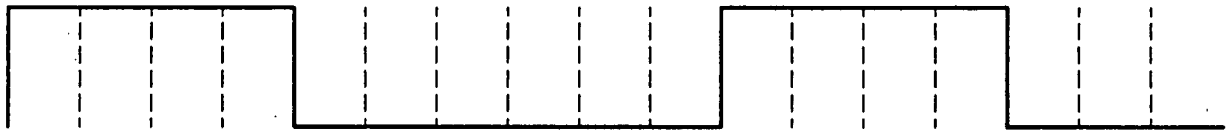
O.G. FIG.
BY DRAFTSMAN | CLASS | SUBCLASS

FIG.21A

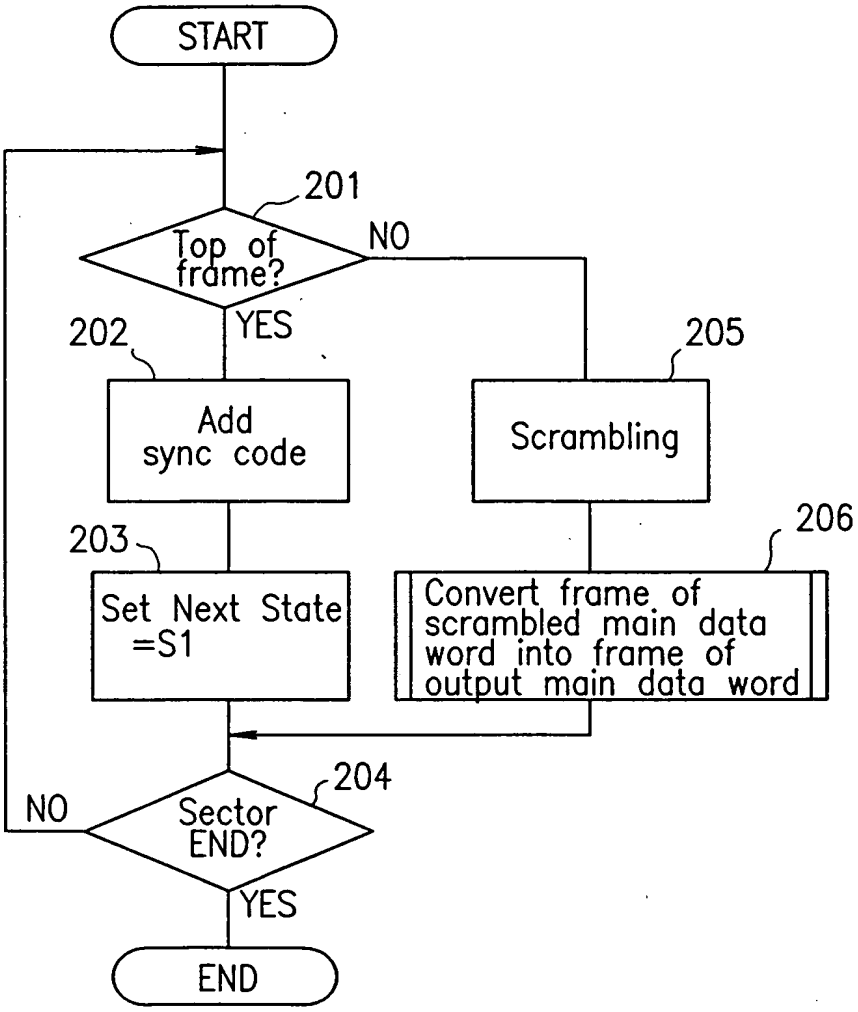
1 0 0 0 1 0 0 0 0 0 1 0 0 0 1 0

FIG.21B



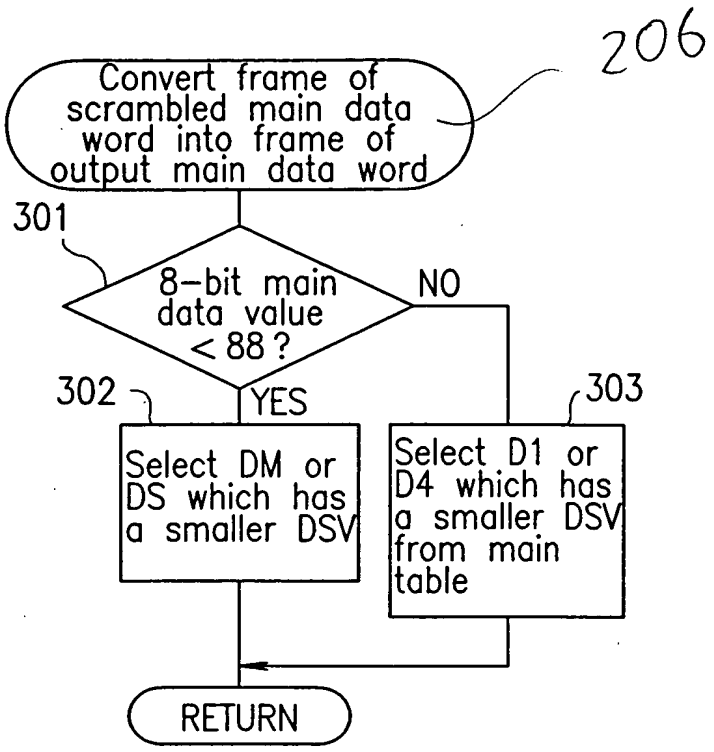
1 1 1 1 0 0 0 0 0 0 1 1 1 1 0 0

FIG. 22



O.G. FIG.
CLASS
SUBCLASS
BY DRAFTSMAN

FIG. 23



O.G. FIG.
CLASS
SUBCLASS
BY
DRAFTSMAN

FIG. 24A

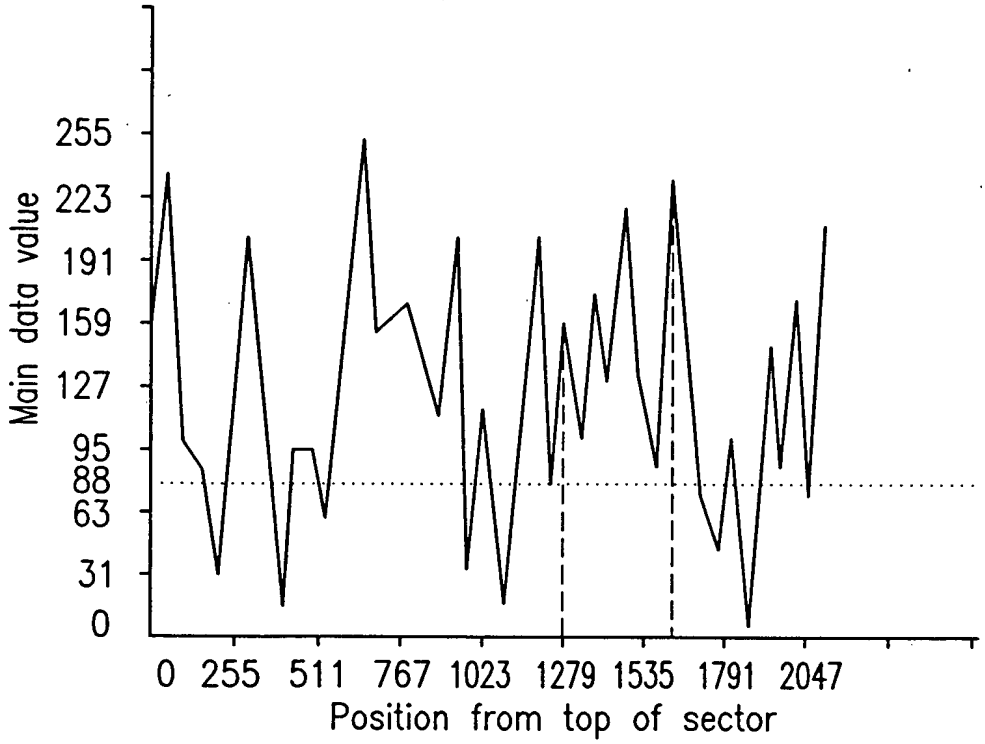
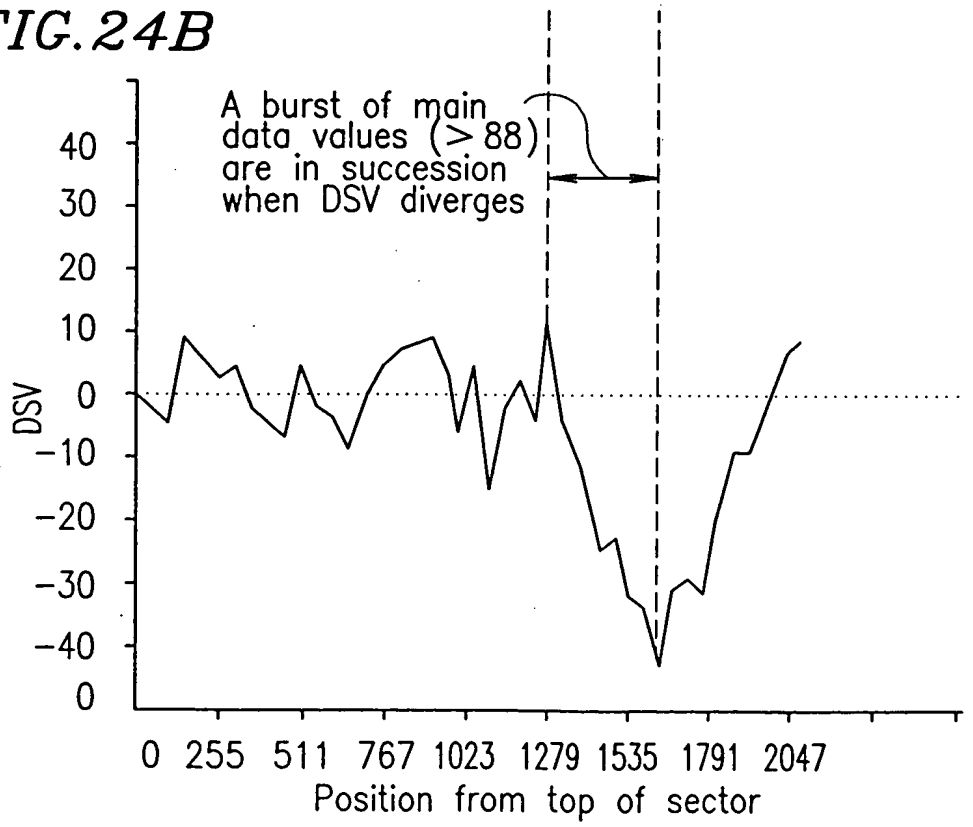



FIG. 24B